Protocol and Performance Analysis of the MPC Parallel Computer

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This paper presents the MPC parallel computer and its MPI implementation performed at the Laboratoire LIP6 of Univ. Pierre and Marie Curie, Paris. MPC is a low cost and high performance parallel computer using standard PC main-boards as processing nodes connected through the specific FastHSL board to a high speed communication network using HSL 1 Gbits/s serial links, IEEE 1355 compliant. Two Asics are presented : RCUBE which is the HSL network router, and PCI-DDC the network controller implementing the Direct Deposit State Less receiver protocol.
The software part of the MPC parallel computer consists of 2 zero-copy layers leading to a latency of 5 to 40µs and a throughput of 490Mbits/s. An efficient MPI implementation based on MPICH is presented and evaluated on an MPC parallel computer. Measures show a latency of 26µs and an useful throughput of 450Mbits/s
This paper presents also a performances study of the MPI implementation on the MPC computer. This reveals several possible optimizations to reduce the overall MPI transfer latency on the MPC Computer.