Restructuration de la mémoire

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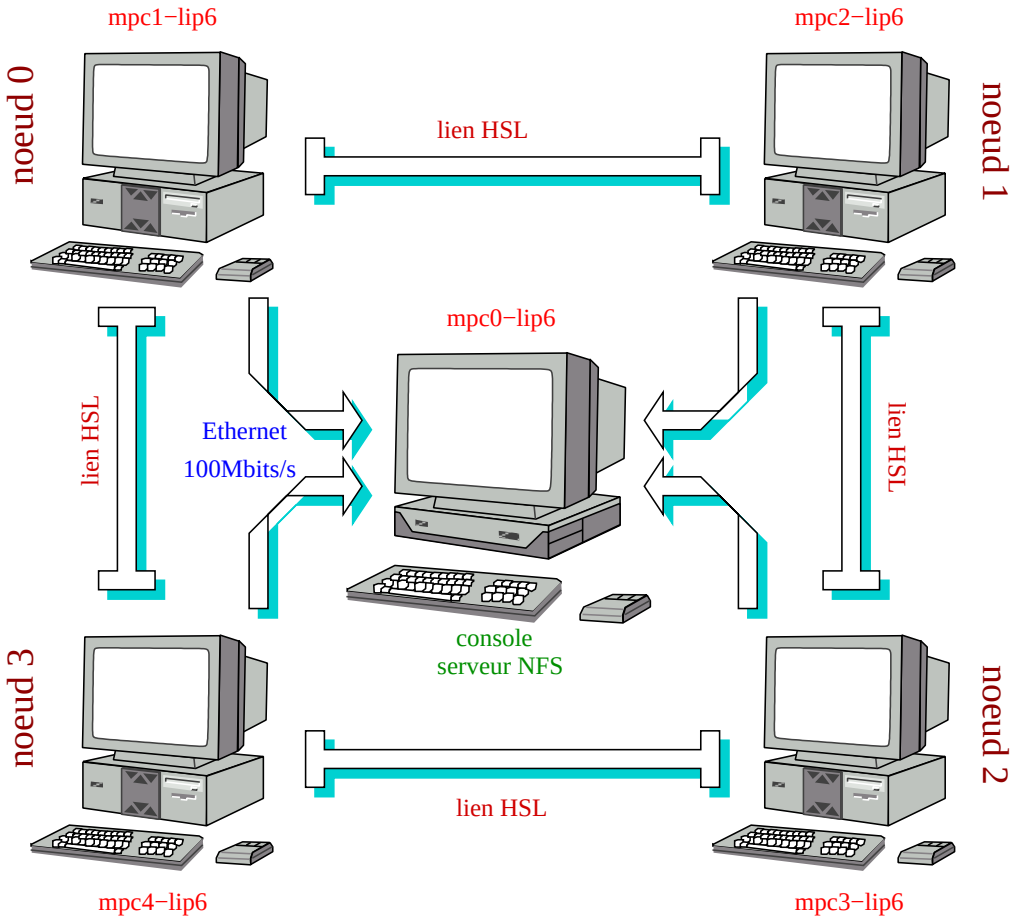

FIG. 1 – Architecture de la machine **MPC**

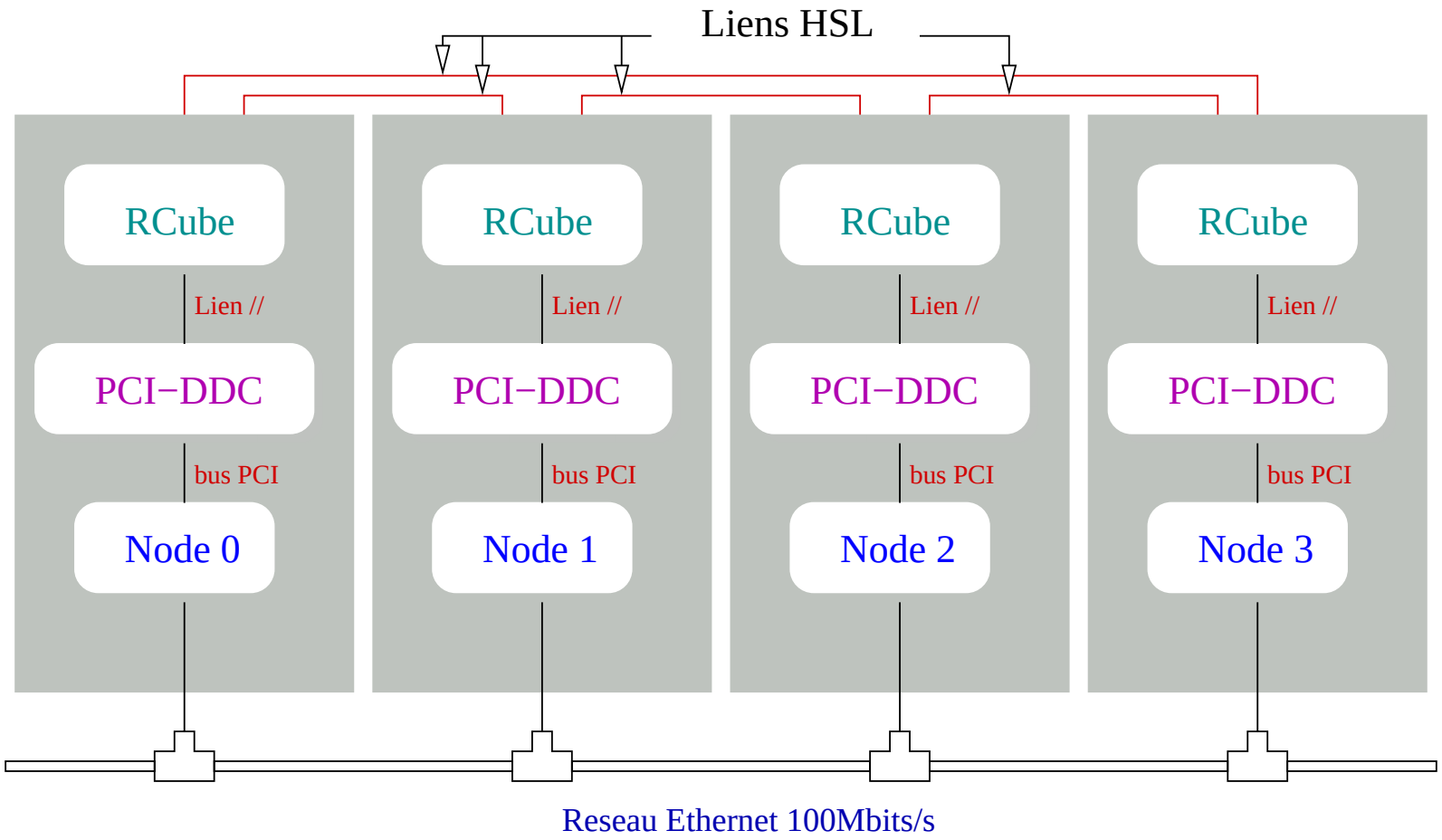

FIG. 2 – Quatre cartes **FastHSL**

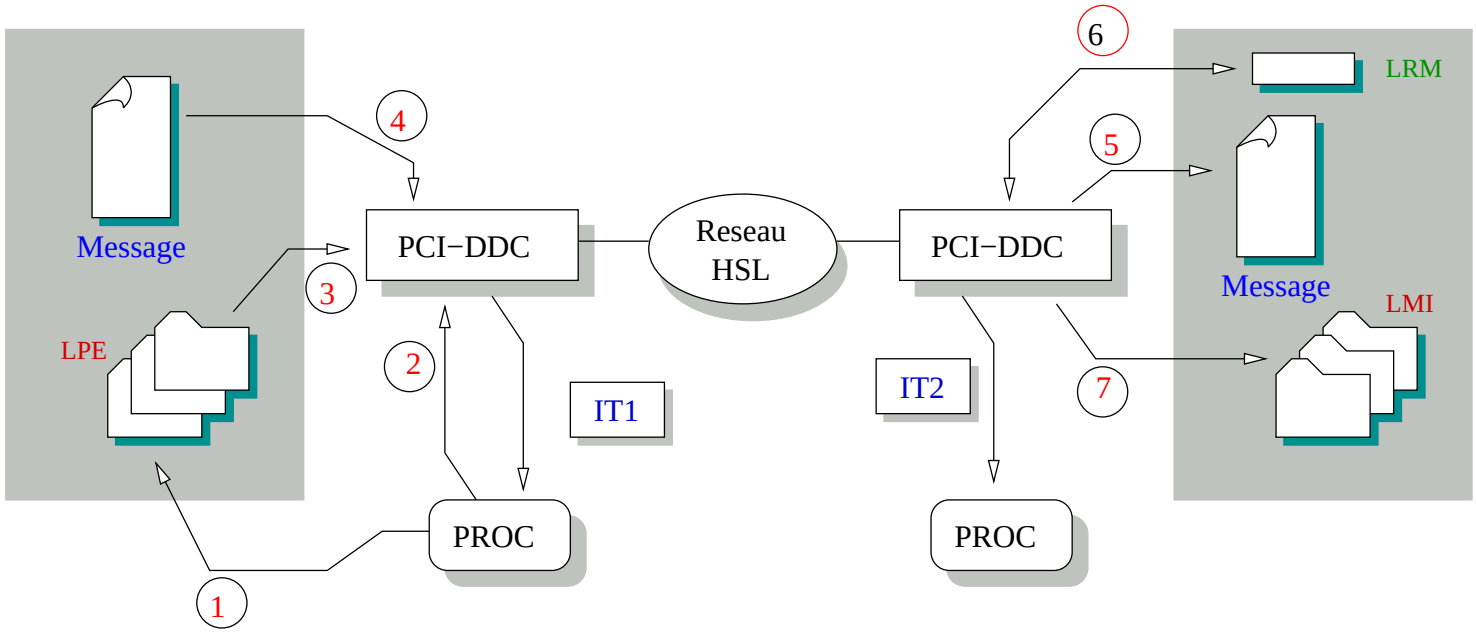

FIG. 3 – Les étapes d'une écriture distante

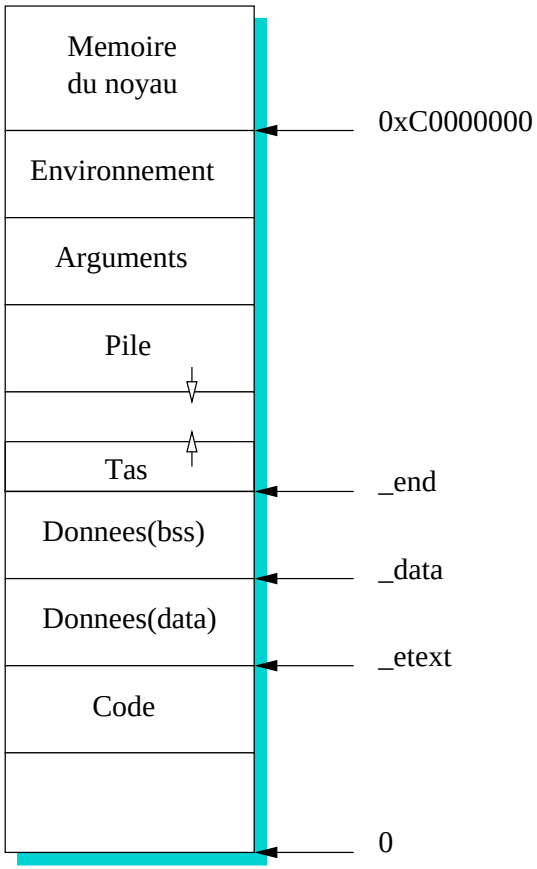

FIG. 4 – Espace d'adressage d'un processus

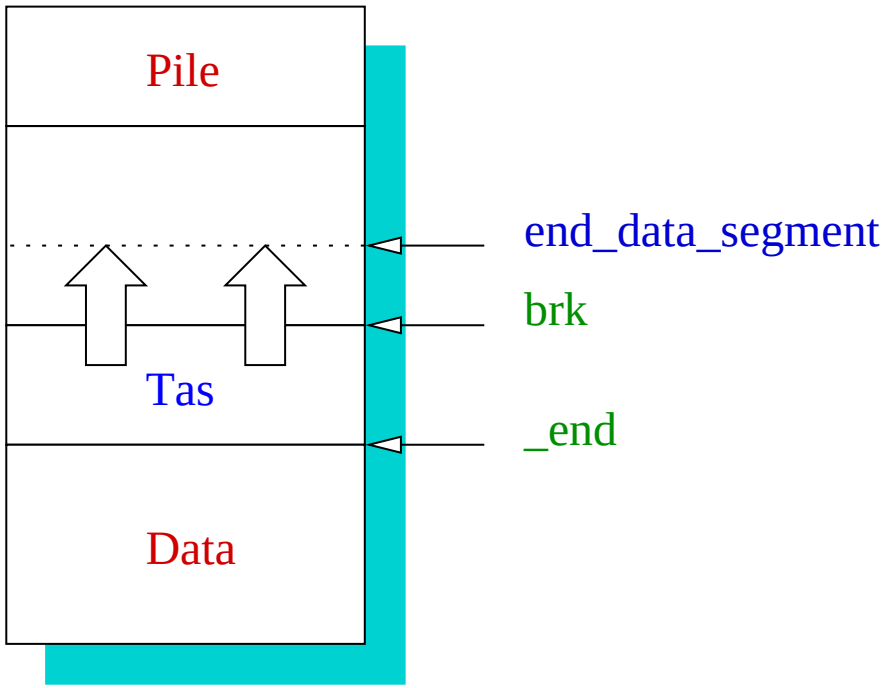

FIG. 5 – Evolution de brk

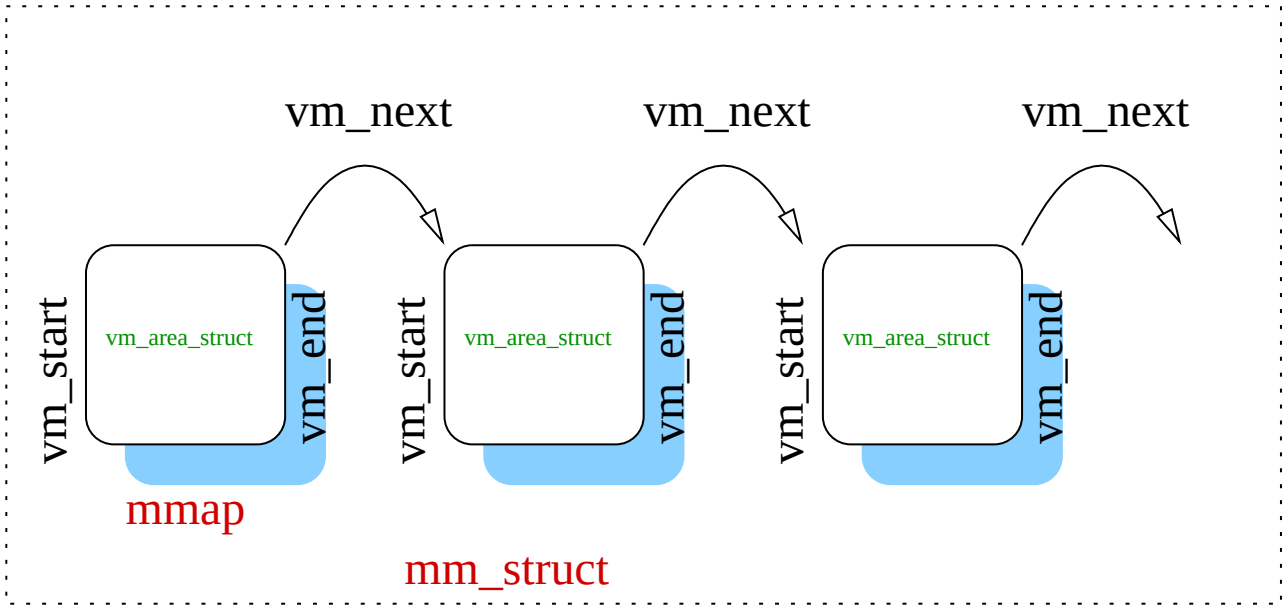

FIG. 6 – Structure mémoire

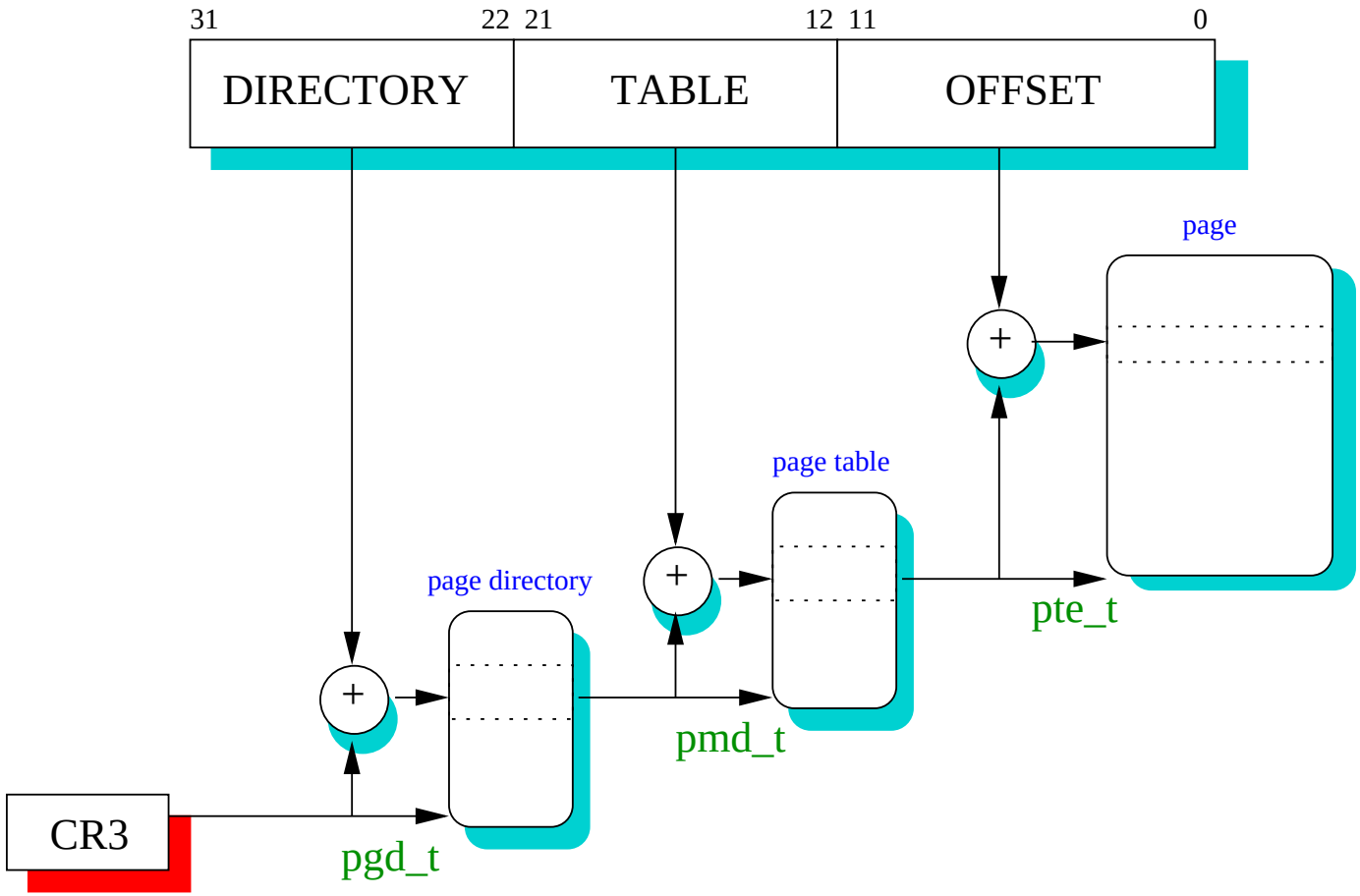

FIG. 7 – Conversion virtuelle physique

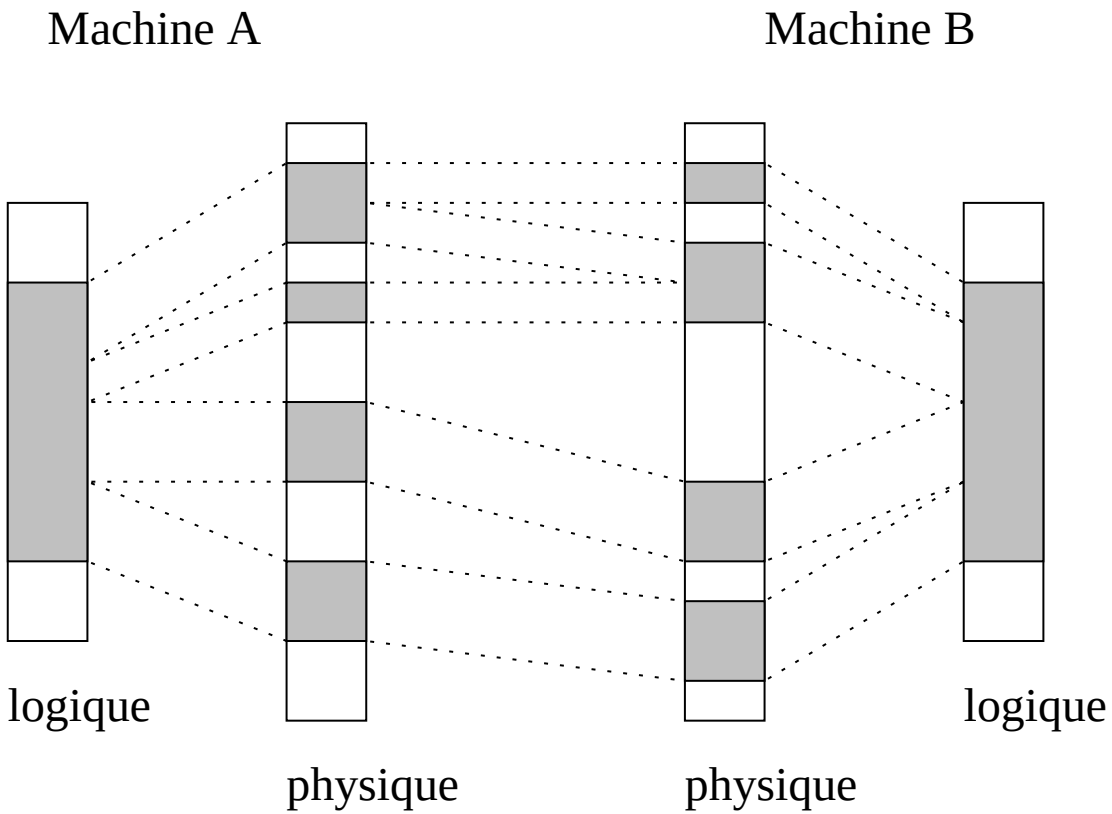

FIG. 8 – transmission discontigüe

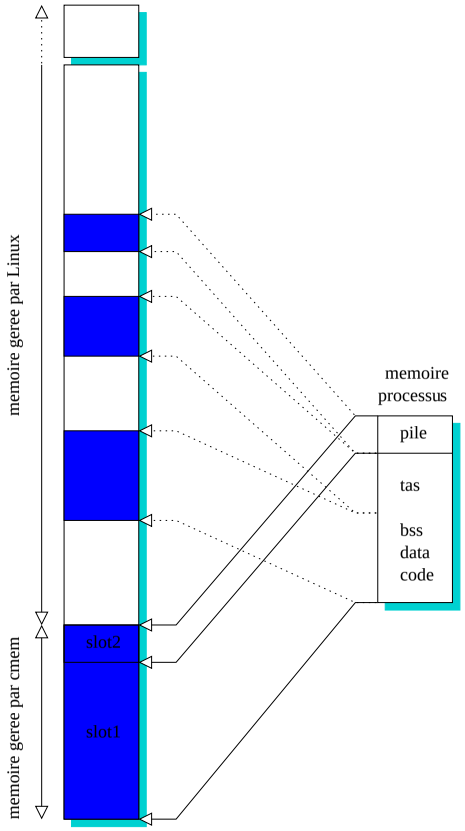

FIG. 9 – Objectif

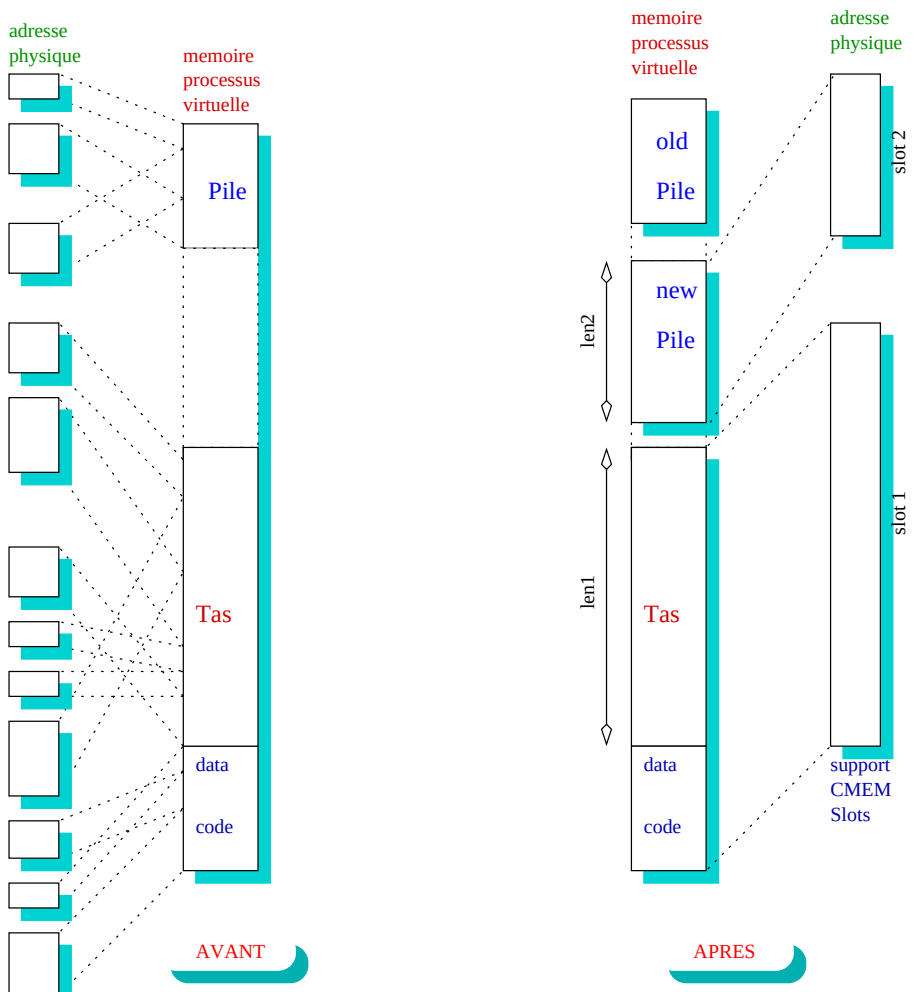

FIG. 10 – Morcellement

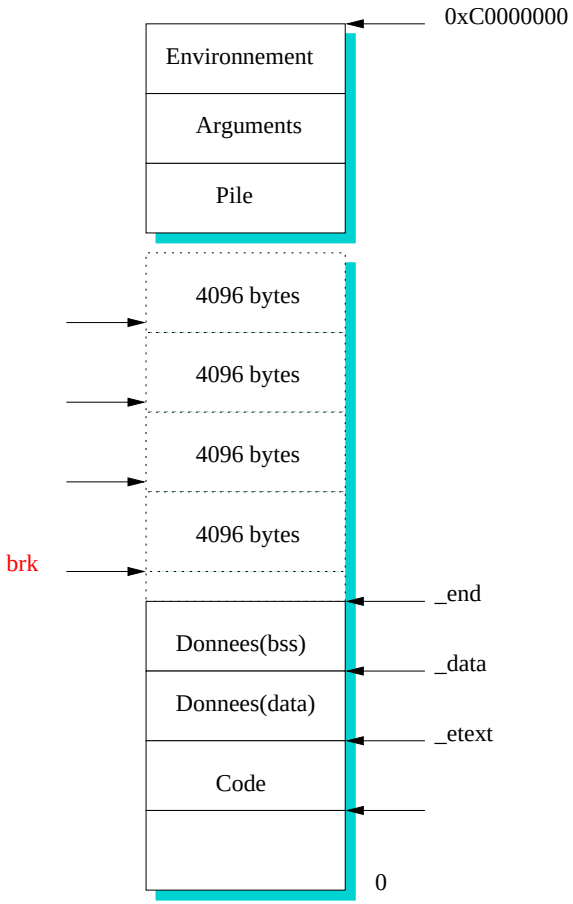

FIG. 11 – Evolution de brk

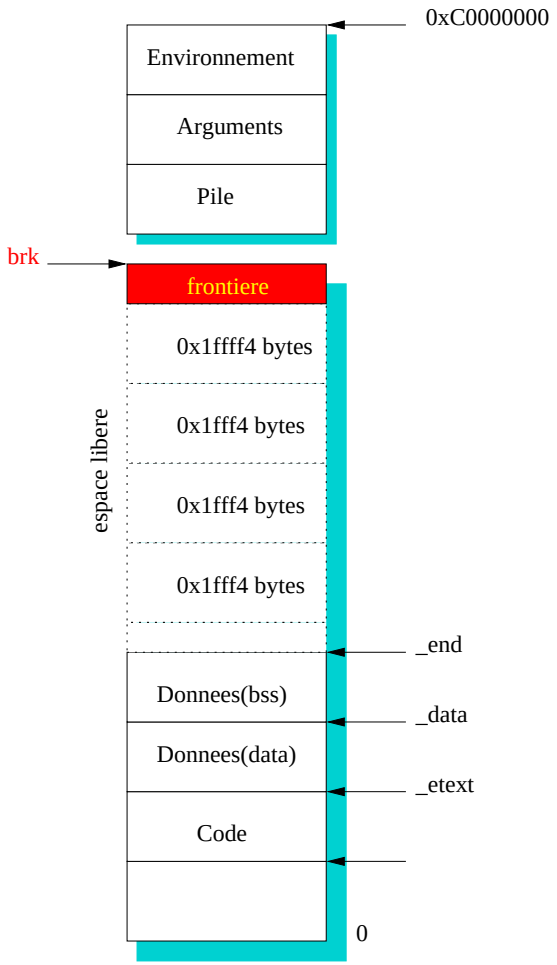

FIG. 12 – Evolution de brk

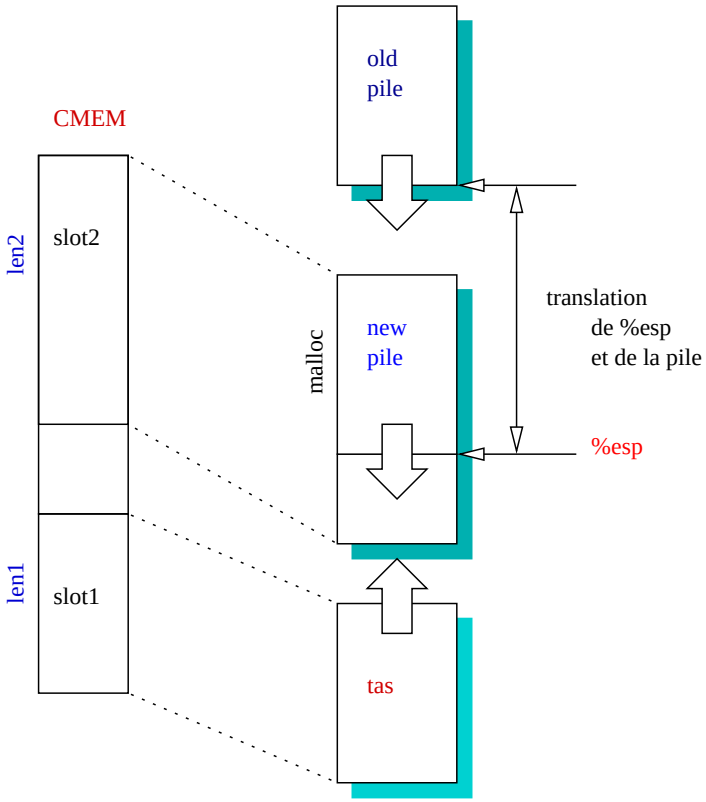

FIG. 13 – Creation de la pile

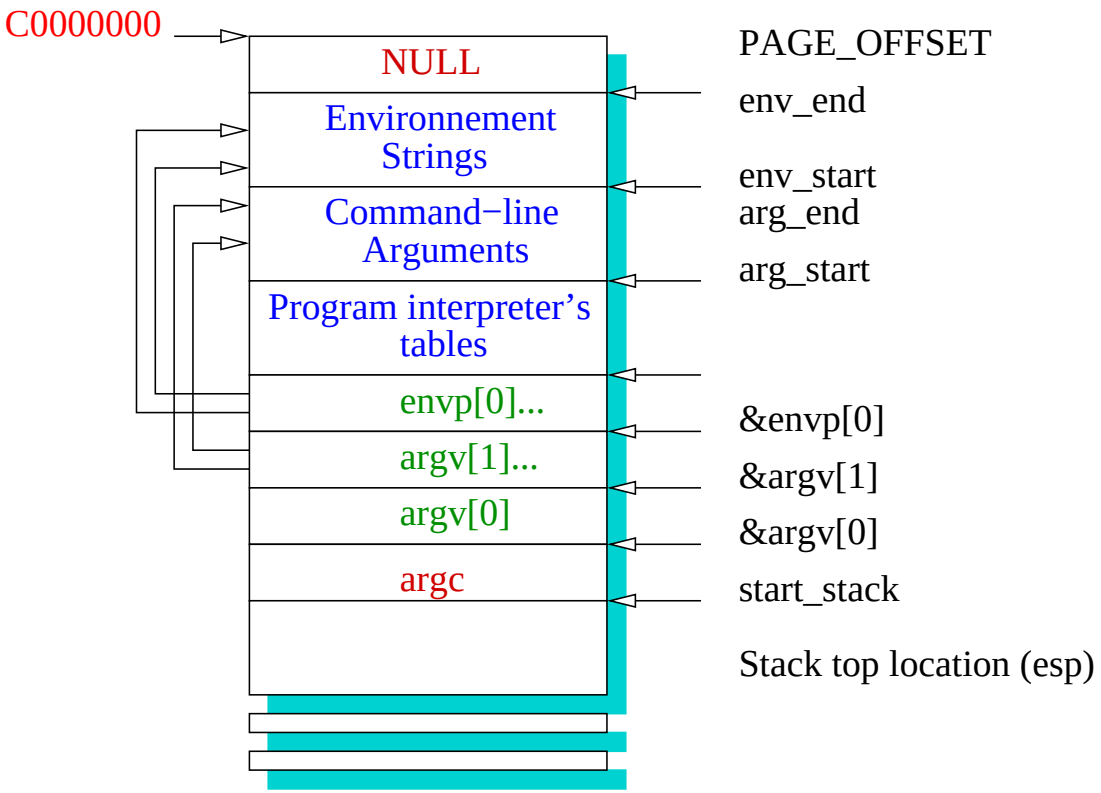

FIG. 14 – Structure du haut de la pile

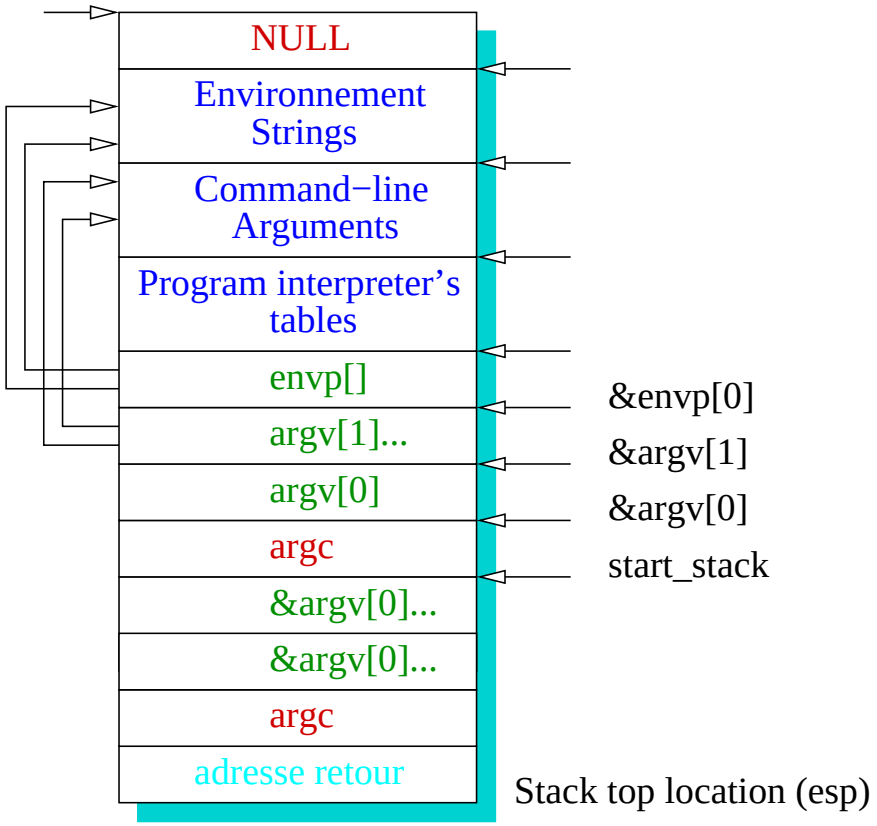

FIG. 15 – Structure de la pile à l'entrée du main

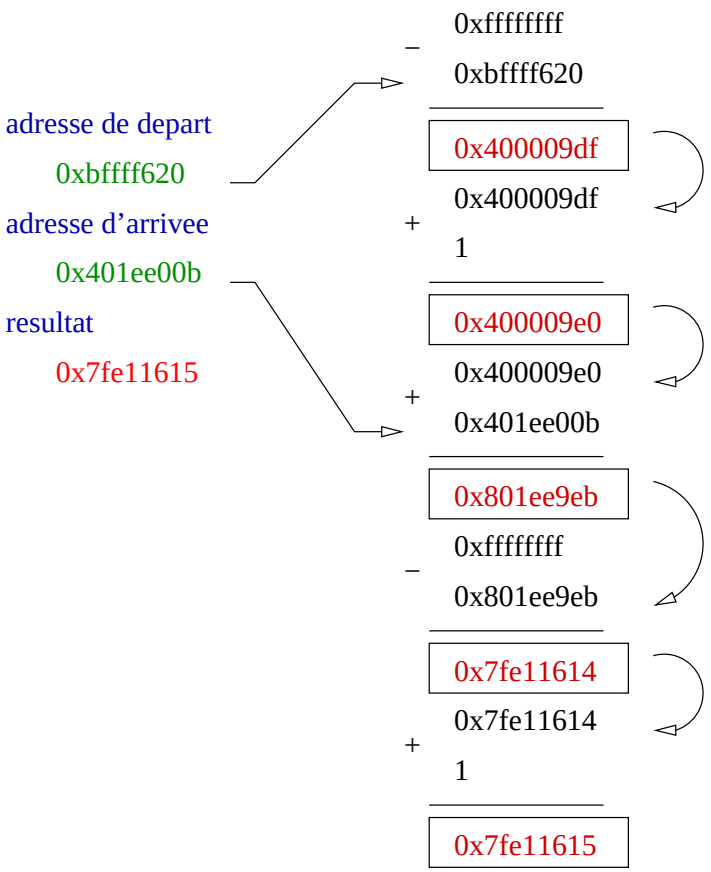

FIG. 16 – Soustraction